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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/640,988	08/14/2003	Andrew W. Lueck	TI-35560	9195

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/640,988	LUECK ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14, 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kelly et al. (US Patent 6,760,793)

As per claim 1, Kelly discloses PCI Express to PCI bridge (fig.9, 901 ie Express-PCI bridge) comprising:

- a PCI interface (fig.9, 931 ie PCI/PCI-X interface) couplable to a PCI bus(fig.9, 933 ie PCI/PCI-X bus) having PCI compatible devices(ie PCI I/O) connected thereto;
- a port arbitration circuit (fig.8, 821 ie switch controller) for controlling the PCI compatible devices to guarantee bandwidth to upstream data sent from a predetermined one of the PCI compatible devices and for allocating the data to a predetermined one of a plurality of virtual channels supported by PCI Express, a virtual channel arbitration circuit for allocating the virtual channels to an output port of the bridge; and (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual

channel, the device assure that it never assigns the device more work tasks than its capacity to handle)

- a PCI Express interface(fig.9, 905, ie serial interface) coupled between the virtual channel arbitration circuit and the output port. (col.9, lines 35-48)

As per claim 2, Kelly discloses the bridge further comprising a port arbitration table (fig.4, 401 ie transactions list) coupled to the port arbitration circuit, the port arbitration table determining PCI bus transactions to guarantee isochronism of data transfers. (col.9, lines 1-34)

As per claim 3, Kelly discloses the bridge further comprising a bus traffic management circuit responsive to the control data stored in the port arbitration table for controlling the port arbitration circuit. (col.9, lines 1-34)

As per claim 4, Kelly discloses the bridge further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to the PCI bus. (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual channel, the device assure that it never assigns the device more work tasks than its capacity to handle)

As per claim 5, Kelly discloses the bridge further comprising a PCI bus arbiter circuit couplable to a PCI bus for controlling access by PCI compatible devices to

the PCI bus. (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual channel, the device assure that it never assigns the device more work tasks than its capacity to handle)

As per claim 6, Kelly discloses wherein the PCI bus arbiter grants control of the PCI bus to a PCI compatible device connected to the bus, the PCI bus arbiter being controlled by the bus traffic management circuit to grant control of the PCI bus to a PCI compatible device sending isochronous data at predetermined intervals to maintain the isochronism of the data. (col.9, lines 1-48)

As per claim 7, Kelly discloses the bridge further comprising an upstream virtual channel window control register, the register being addressed by a PCI compatible device for sending isochronous data. (col.9, lines 1-48)

As per claim 8, Kelly discloses wherein the window control register is located within PCI Express configuration space. (col.9, lines 1-48)

As per claim 9, Kelly discloses wherein the window control register is located within extended PCI configuration space. (col.9, lines 1-48)

As per claim 10, Kelly discloses wherein the window control register is located in memory. (col.9, lines 1-48)

As per claim 11, Kelly discloses wherein the memory is located within the bridge.(col.9, lines 1-48, figure 8)

As per claim 12, Kelly discloses wherein the memory is located in memory mapped configuration space. (col.9, lines 1-48, figure 8)

As per claim 13, Kelly discloses the bridge further comprising a virtual channel arbitration circuit. (col.9, lines 1-48, figure 8)

As per claim 14, Kelly discloses wherein the upstream data is isochronous data. (col.9, lines 1-48, figure 8)

As per claim 16, Kelly discloses a method for isochronous transfer of data from a PCI compatible device connected to a PCI bus to a PCI Express fabric comprising:

- receiving data at an input port for isochronous transfer from a preselected PCI compatible device; (col.9, lines 1-48)
- controlling PCI compatible devices on the PCI bus to guarantee bandwidth from the preselected PCI device; (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual channel,

the device assure that it never assigns the device more work tasks than its capacity to handle)

- allocating the data from the preselected device to one of a plurality of virtual channels supported by PCI Express; (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual channel, the device assure that it never assigns the device more work tasks than its capacity to handle)
- arbitrating the virtual channels onto an output port. (col.9, lines 1-48)

As per claim 17, Kelly discloses wherein controlling PCI compatible devices on the PCI bus is in response to control signals generated in response to a port arbitration table. (col.9, lines 1-48)

As per claim 18, Kelly discloses the method further comprising: writing data from a PCI compatible device to a register defined in a PCI Express to PCI bridge to define the data transfer as isochronous. (col.9, lines 1-48)

As per claim 19, Kelly discloses a method for isochronous transfer of data between a PCI compatible device and PCI Express fabric comprising:

- receiving data from a PCI compatible device connected to a PCI bus, the data being addressed to a register defined in a PCI Express to PCI bridge; (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set

for each port for each virtual channel, the device assure that it never assigns the device more work tasks than its capacity to handle)

- transferring the data addressed to the register upstream to a PCI Express fabric, the data transfer maintaining isochronism of the data. (col.9, lines 1-48)

As per claim 20, Kelly discloses a PCI Express to PCI bridge comprising:

- first means for receiving data from a PCI compatible device connected to a PCI bus and sending the data upstream to a CPU via a PCI Express fabric, the first means maintaining isochronism of isochronous data from the PCI compatible device, and (col.7, line 17-col.8, line 67, ie switch sets the input and output buffer set for each port for each virtual channel, the device assure that it never assigns the device more work tasks than its capacity to handle)
- second means for receiving isochronous data from the CPU via the PCI Express fabric and for sending the data downstream to the PCI compatible device, the second means maintaining isochronism of the data.(col.9, lines 1-48)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Patent 6,760,793) in view of Hewitt et al. (US Patent 6,199,132)

Kelly discloses all the limitations as above except wherein the PCI compatible device is an IEEE 1394 device. However, Hewitt discloses I/O module can include expansion link, IEEE1394, or PCI which can provide guaranteed bandwidth to each isochronous stream. (col.3, lines 9-26)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hewitt's teaching into Kelly's system so as to reduce latency for transfer of data in order to improve system performance. (col.1, lines 56-58)

Conclusion

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

September 30, 2005

Khanh Dang
Primary Examiner